IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Rule 53(b) Divisional Application of:

IKEMASU et al.

Divisional of S.N. 08/876,908 filed June 16, 1997 Group Art Unit: To Be Assigned

Filed: Herewith Examiner: To Be Assigned

For: HIGHLY INTEGRATED AND RELIABLE DRAM ADAPTED FOR SELF-ALIGNED-CONTACT (As Amended)

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

August 3, 2001

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 20-61without prejudice or disclaimer.

Please amend claims 1 and 3 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film of metal or metal silicide, a first insulating film, and a third insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of second insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the second insulating film being made of a same material as the first insulating film, and having a thickness smaller than that of the first insulating film;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said second insulating films, to be contiguous to said third insulating film, the third and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said third and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

3. (Amended) A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film made of metal or metal silicide, a first insulating film, and a third insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of second insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the second insulating film having a thickness smaller than that of the first insulating film, the first and second insulating films being made of different materials except silicon nitride;

a pair of fourth insulating films formed on the pair of side walls of the lamination through

said second insulating films, to be contiguous to said third insulating film, the third and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said third and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

Please add claims 62-79 as follows:

62. A semiconductor device according to claim 3, wherein said second insulating film extends under a bottom end of said fourth insulating film positioned on the side wall of said lamination.

63. A semiconductor device according to claim 3, wherein said conductive pattern is a gate electrode of a MIS transistor.

64 A semiconductor device according to claim 3, wherein said second insulating film is made of a silicon oxide film.

65. A semiconductor device according to claim 3, wherein said interlevel insulating layer has etching characteristics different from a silicon nitride film and is formed on said third insulating film made of a silicon nitride.

66. A semiconductor device according to claim 1, wherein said conductive pattern forms a bit line of dynamic random access memory.

67. A semiconductor device according to claim 3, wherein said conductive pattern forms a bit line of dynamic random access memory.

68. A semiconductor device according to claim 3, wherein the first insulating film is made of silicon oxy-nitride.

69. A semiconductor device according to claim 3, wherein the surface of said interlevel insulating layer is generally parallel to said semiconductor substrate.

70. A semiconductor device according to claim 65, further comprising:

a conductive plug filling the contact area.

71. A semiconductor device according to claim 70, further comprising:

a fifth insulating film formed on the interlevel insulation layer and defining a contact area on said conductive plug.

72. A semiconductor device according to claim 71, further comprising:

an upper conductive pattern formed on said fifth insulating film and on said conductive plug;

a sixth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a seventh insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said sixth insulating film.

73. A semiconductor device according to claim 72, further comprising:

another contact area formed in said interlevel insulating layer on an opposite side of said conductive pattern to said contact area, having a bottom portion at least partially defined by said fourth insulating film; and

another conductive plug filling said another contact area;

wherein said fifth insulating film further defines another contact area on said another conductive plug.

74. A semiconductor device according to claim 73, further comprising a storage capacitor formed on said another conductive plug.

75. A semiconductor device according to claim 74, wherein said storage capacitor is formed to at least partially cover said seventh insulating film.

76. A semiconductor device according to claim 75, further comprising:

an eighth insulating film made of silicon nitride, formed between said fourth and fifth insulating films, and cooperatively defining said contact area with said fourth insulating film.

77. A semiconductor device according to claim 76, further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film and on said fifth insulating film; and

silicon nitride layers covering said wiring patterns.

78. A semiconductor device according to claim 77, further comprising:

an interlayer insulating layer covering said fifth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said fifth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns.

79. A semiconductor device according to claim 78, wherein said storage capacitor includes a storage electrode connected to said another conductive plug, a dielectric film formed on said storage electrode and on said fifth insulating film, and an opposing electrode formed on said dielectric film having an extension on said fifth insulating film, one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.

REMARKS

Claims 1-19 and 62-79 are pending. Claims 20-61 are cancelled, claims 1 and 3 are amended, and new claims 62-79 are added. Prompt and favorable action on the merits is earnestly solicited.

Attached hereto is a marked-up version of the changes made to the claims. The attached page is captioned "**Version with markings to show changes made.**"

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: (1) Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 3 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating [surface] film;

[a conductive pattern disposed on the insulating surface of said semiconductor substrate, said conductive pattern including at least one layer of metal or metal silicide;

a first insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said conductive pattern; and

a second insulating film made of silicon nitride formed to continuously cover said conductive pattern and said first insulating film]

lamination of a first conductive film of metal or metal silicide, a first insulating film, and a third insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of second insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the second insulating film being made of a same material as the first insulating film, and having a thickness smaller than that of the first insulating film;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said second insulating films, to be contiguous to said third insulating film, the third and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said third and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

3. (Amended) A semiconductor device [according to claim 2, wherein the first insulating film on the side wall of said conductive pattern is a different film from said first insulating film on the upper surface of said conductive pattern] comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film made of metal or metal silicide, a first insulating film, and a third insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of second insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the second insulating film having a thickness smaller than that of the first insulating film, the first and second insulating films being made of different materials except silicon nitride;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said second insulating films, to be contiguous to said third insulating film, the third and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said third and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.